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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/713,389	11/15/2000	John E. Gavlik	P04761	3470

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EXAMINER

EL CHANTI, HUSSEIN A

ART UNIT	PAPER NUMBER
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2157

DATE MAILED: 12/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/713,389

Applicant(s)

GAVLIK ET AL.

Examiner

Hussein A. El-chanti

Art Unit

2157

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 September 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7,9-15 and 17-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7,9-15 and 17-25 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This action is responsive to amendment received on Sep. 26, 2005.

Claims 1, 9 and 17 were amended. Claims 8 and 16 were canceled. Claims 23-25 were newly added. Claims 1-7, 9-15 and 17-25 are pending examination.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 24 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 24 is dependent on claim 8 which was cancelled.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5, 8-13, 16-21 and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Johnston et al., U.S. Patent No. 5,781,776 (referred to hereafter as Johnston).

As to claim 1, Johnston teaches an apparatus for controlling a physical layer interface of a network interface card, said apparatus comprising:

a read only memory (ROM) capable of storing an embedded control program (see col. 5 lines 25-67, microcontroller has a ROM that stores the control program);

a random access memory capable of storing a downloadable software control program downloaded from an external processing system (see col.5 lines 25-67, upgrades to the control program may be downloaded to a RAM); and

a microcontroller capable of controlling said physical layer interface, wherein said microcontroller in a first operating mode is capable of executing said embedded control program to thereby control said physical layer interface, and wherein said microcontroller in a second operating mode is capable of executing said downloadable software control program in place of said embedded control program to thereby control said physical layer interface (see col. 7 line 55-col.8 line 66, control program is updated by downloading new program instructions);

wherein said microcontroller comprises a plurality of control registers capable of controlling said first and second operating modes, wherein said microcontroller switches from said first operating mode to said second operating mode when said external processing system stores a jump address to said RAM in a first one of said plurality of control registers (see col.7 line 55-col.8 line 66, the new instructions are executed by installing a branch or jump instruction to execute the new program stored on the new memory location).

As to claim 9, Johnston teaches a processing system comprising:

a data processor;

a hard disk drive capable of storing thereon a network interface card (NIC) configuration file containing a downloadable software control program; and

a network interface card for coupling said processing system to a data network, said network interface card comprising:

an apparatus for controlling a physical layer interface of said network interface card, said apparatus comprising:

a read only memory (ROM) capable of storing an embedded control program (see col. 8 lines 12-30 and col. 12 lines 35-47);

a random access memory capable of storing a downloadable software control program (see col. 8 lines 12-30 and col. 12 lines 35-47); and

a microcontroller capable of controlling said physical layer interface, wherein said microcontroller in a first operating mode executes said embedded control program to thereby control said physical layer interface, and wherein said microcontroller in a second operating mode is capable of downloading said downloadable software control program from an external processing system and executing said software control program in place of said embedded control program to thereby control said physical layer interface (see col. 8 lines 12-30, col. 12 lines 35-47 and col. 13 lines 59-65, the control program is downloaded to the RAM or EPROM where the start address is changed to start at the address of the control program loaded on the memory external to the internal ROM).

As to claim 17, Johnston teaches a physical layer interface controllable by a microcontroller embedded therein, a method of operating the microcontroller comprising the steps of:

in a first operating mode, executing an embedded control program stored in a read only memory (ROM) coupled to the microcontroller to thereby control the physical layer interface (see col. 8 lines 12-30 and col. 12 lines 35-47);

in a second operating mode, downloading a software control program from an external processing system and storing the software control program in a random access memory (RAM) coupled to the microcontroller and, in response to the step of downloading the software control program, executing the software control program in place of the embedded control program to thereby control the physical layer interface (see col. 8 lines 12-30, col. 12 lines 35-47 and col. 13 lines 59-65, the control program is downloaded to the RAM or EPROM where the start address is changed to start at the address of the control program loaded on the memory external to the internal ROM).

As to claims 2, 10 and 18, Johnston teaches the apparatus, system and method as set forth in Claims 1, 9 and 17 respectively wherein said ROM is an internal ROM in said microcontroller (see figure 2, col. 5 lines 25-67).

As to claims 3, 11 and 19, Johnston teaches the apparatus, system and method as set forth in Claims 1, 9 and 17 respectively wherein said RAM is an internal RAM in said microcontroller (see figure 2, col. 5 lines 25-67).

As to claims 4, 12 and 20, Johnston teaches the apparatus, system and method as set forth in Claims 1, 9 and 17 respectively wherein said ROM is an external ROM coupled to said microcontroller (see figure 2, col. 5 lines 25-67).

As to claims 5, 13 and 21, Johnston teaches the apparatus, system and method as set forth in Claim 1, 9 and 17 respectively wherein said RAM is an external RAM coupled to said microcontroller (see figure 2, col.5 lines 25-67).

As to claim 24, Johnston teaches first control register comprises a last register in a first register filed in the microcontroller (see col.7 lines 28-67).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 6-7, 14-15 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnston in view of Williams, U.S. Patent No. 6,859,825.

As to claims 6-7, 14-15 and 22-23, Johnston teaches a microcontroller capable of controlling said physical layer interface, wherein said microcontroller in a first operating mode executes said embedded control program to thereby control said physical layer interface, and wherein said microcontroller in a second operating mode is capable of downloading said downloadable software control program from an external processing system and executing said software control program in place of said embedded control

program to thereby control said physical layer interface col. 8 lines 12-30, col. 12 lines 35-47 and col. 13 lines 59-65 and fig. 7).

Johnston does not explicitly teaches the downloading control program via MDC and MDIO via MAC. However Williams teaches a system and method for downloading program to configure a MAC via a MDC/MDIO signal path (see col. 5 lines 5-25).

It would have been obvious for one of the ordinary skill in the art at the time of the invention to modify Johnston by downloading control program using a MDC/MDIO signal because doing so would allow the MDIO logic 42 determines the address for the PHY and the address for the register from the prescribed configuration information and then sends the information to the appropriate controller via a shared management databus (see col. 5 lines 5-25).

Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Johnston.

Johnston does not explicitly teach the microcontroller includes 256 registers, each register filed containing 32 16-bit registers. Official Notice is taken that one of ordinary skill in the art, would use 256 registers, each register filed containing 32 16-bit registers; because doing so would result in executing the updated control program that is taught by Johnston.

4. Applicant's arguments have been fully considered but are moot in view of the new grounds of rejection.

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hussein A. El-chanti whose telephone number is (571)272-3999. The examiner can normally be reached on Mon-Fri 8:30-5:00.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ario Etienne can be reached on (571)272-4001. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2157

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hussein El-chanti

Dec. 21, 2005


ARTO ETIENNE
SUPERVISORY PATENT EXAMINER
EBC TECHNOLOGY CENTER 2100